More CUDA Accelerated LTL Model Checking

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D3S Seminar based on
CUDA accelerated LTL Model Checking
[Barnat et al. ICPADS'09]

DiVinE-CUDA – A Tool for GPU Accelerated LTL Model Checking
[Barnat et al. PDMC’09]

Employing Multiple CUDA Devices to Accelerate LTL Model Checking
[Barnat et al. ICPADS’10]

CUDA Accelerated LTL Model Checking – Revisited
[Bauch et al. MEMICS’10]

18.1, 2011
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Motivation

Formal verification

- critical system - any mistake may have fatal consequences
- testing is insufficient - can not guarantee correctness
- formal methods can prove or disprove correctness of the system
Motivation

Formal verification

- critical system - any mistake may have fatal consequences
- testing is insufficient - can not guarantee correctness
- formal methods can prove or disprove correctness of the system

Model Checking

- fully automated approach to the formal verification
- state space explosion problem
- possible solution:
  - symbolic representation
  - reduction techniques
  - platform-dependent verification
Platform-dependent Verification

DiVinE

• Explicit Parallel LTL Model Checker
• Focuses on full utilization of available HW power
Platform-dependent Verification

DiVinE

- Explicit Parallel LTL Model Checker
- Focuses on full utilization of available HW power

Successful stories on the following parallel platforms

- Clusters, Grids
  DiVinE Cluster
- Multi-core workstations
  DiVinE Multi-Core
- Cluster of Multi-core workstations
  DiVinE 2.x
Platform-dependent Verification

**DiVinE**

- Explicit Parallel LTL Model Checker
- Focuses on full utilization of available HW power

**Successful stories on the following parallel platforms**

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  - DiVinE Multi-Core
- Cluster of Multi-core workstations
  - DiVinE 2.x

**Many-core architectures**

- Shared-memory setting, many computing cores
- Parallel computing platform of the future?
- Widely accessible due to GP GPU devices
Many-core Architecture

NVIDIA CUDA Technology

- Many-core architecture
- Hundreds of computing cores
- HW support for thousands of computing threads
- Requires quite specific memory-usage pattern
- Incompatible with random memory access (hashing)
- Limited size of the GPU memory
Many-core Architecture

NVIDIA CUDA Technology

- Many-core architecture
- Hundreds of computing cores
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Need for new many-core algorithms

- Straightforward adaptation of distributed and multi-core algorithms to many-core architecture is inefficient
- Necessity of expensive phase of construction of data structures
- Partitioning of data structures for multiple device computation
- Also the case of parallel LTL Model Checking
Previous solution

- successful redesign of MAP algorithm – significant GPU acceleration [Barnat et al. ICPADS'09]
- DiVinE-CUDA – tool for CUDA Accelerated LTL Model Checking [Barnat et al. PDMC’09]

Two weaknesses of our approach

- expensive phase of encoding the state space into the suitable representation
- limited to the middle-size instances that can fit the memory of a single CUDA device
Solution of the weaknesses

[Barnat et al. ICPADS’10]

- multi-core acceleration of expensive encoding the state space into the CSR representation
- overcoming of single GPU memory limitations
- verification of much larger model checking problems
- preserving a decent efficiency of our inter-CUDA communication intensive parallel algorithm
Solution of the weaknesses

[Barnat et al. ICPADS’10]
- multi-core acceleration of expensive encoding the state space into the CSR representation
- overcoming of single GPU memory limitations
- verification of much larger model checking problems
- preserving a decent efficiency of our inter-CUDA communication intensive parallel algorithm

[Bauch et al. MEMICS’10]
- redesign of the OWCTY algorithm
- significantly outperform the original CUDA MAP algorithm
- robust to improper ordering in the input representation
LTL Model Checking

Model Checking

Does the model $M$ satisfy the formula $\varphi$?

Inspected system $\rightarrow$ Model $M$  
Formula $\varphi$ $\rightarrow$ Required property

Yes, $M$ satisfies $\varphi$   
No, $M$ does not satisfy $\varphi$  
(counter example)
LTL Model Checking

Model Checking

Does the model $M$ satisfy the formula $\varphi$?

Inspected system $\rightarrow$ Model $M$ $\quad$ Formula $\varphi$ $\rightarrow$ Required property

Yes, $M$ satisfies $\varphi$  No, $M$ does not satisfy $\varphi$

(counter example)

LTL Model Checking

- required property $\rightarrow$ formula in Linear Temporal Logic (LTL)
- examples: $\varphi = FG(p)$ – from certain moment $p$ always holds
  $\varphi = G(p \Rightarrow F(q))$ – response
LTL Model Checking

Model Checking

Does the model $M$ satisfy the formula $\varphi$?

Inspected system $\rightarrow$ Model $M$  
Formula $\varphi$ $\leftarrow$ Required property

Yes, $M$ satisfies $\varphi$  
No, $M$ does not satisfy $\varphi$ (counter example)

LTL Model Checking

- required property $\rightarrow$ formula in Linear Temporal Logic (LTL)
  - examples: $\varphi = FG(p)$ – from certain moment $p$ always holds  
  $\varphi = G(p \Rightarrow F(q))$ – response

Solution

- automata based approach
- reduction on accepting cycle detection
Algorithms for Accepting Cycle Detection

- Optimal time complexity but hard to parallelize:
  - Nested DFS
  - Tarjan's SCC decomposition

- Unoptimal time complexity but easy to parallelize:
  - One-Way-Catch-Them-Young (OWCTY)
  - Maximal accepting predecessor (MAP)
Algorithms for Accepting Cycle Detection

Optimal time complexity but hard to parallelize:
- Nested DFS
- Tarjan’s SCC decomposition
Algorithms for Accepting Cycle Detection

Optimal time complexity but hard to parallelize:
- Nested DFS
- Tarjan’s SCC decomposition

Unoptimal time complexity but easy to parallelize:
- One-Way-Catch-Them-Young (OWCTY)
- Maximal accepting predecessor (MAP)
Algorithm MAP

Graph corresponding to the state space.
Algorithm MAP

Accepting vertices, accepting cycle.
Algorithm MAP

4 > 2 > 1 6 5
3 4

Vertex ordering.
Maximal Accepting Predecessor (MAP)

\[ map(v) = \max\{\bot, u \mid (u, v) \in E^+ \land A(u)\} \]
Algorithm MAP

\[
\text{map}(v) = v \implies \text{accepting cycle}
\]
Algorithm MAP

What if $2 > 4$?
Algorithm MAP

Accepting cycle undetected.
If no accepting cycle is found, then maximal accepting vertices cannot be part of an accepting cycle.
Maximal accepting vertices marked as non-accepting.
Algorithm MAP

Repeat until accepting cycle is found or there are no accepting vertices.
Computing Values of MAP – Many-cores

One thread per vertex.
Computing Values of MAP – Many-cores

Each thread processes all incoming edges.
Computing Values of MAP – Many-cores

Threads proceed simultaneously.
Computing Values of MAP – Many-cores

Threads proceed simultaneously.
Computing Values of MAP – Many-cores

Accepting cycle found.
MAP Algorithm as Matrix-Vector Product

$$M \times V = V'$$
MAP Algorithm as Matrix-Vector Product

\[ V'[i] = \sum_{0 \leq j \leq n} M[i][j] \cdot V[j] \]
MAP Algorithm as Matrix-Vector Product

\[
V'[i] = \sum_{0 \leq j \leq n} M[i][j] \cdot V[j]
\]

\[
V'[i] = \max_{0 \leq j \leq n} M[i][j] \cdot \maxacc(V[j], i)
\]

\[
\text{maxacc}(u, v) = \begin{cases} 
\max\{\text{map}(u), \text{map}(v), u\} & \text{if } A(u) \\
\max\{\text{map}(u), \text{map}(v)\} & \text{otherwise.}
\end{cases}
\]
Two Weaknesses of our Approach

1. Expensive construction of the CSR representation
   - handling full matrices of predecessors is memory inefficient
   - Compact Sparse Row (CSR) representation of the graph

\[
\begin{pmatrix}
1 & 0 & 1 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 1
\end{pmatrix}
\]

\[\text{Mc} = (0 \ 2 \ 1 \ 4 \ 3 \ 1 \ 0 \ 4)\]
\[\text{Mr} = (0 \ 2 \ 4 \ 5 \ 6)\]

- CSR construction takes 93% of total verification time
Parallel Construction of CSR Representation

**Basic idea**

1. Multi-core parallel state space generation

   - hash-based partitioning of the graph
   - local storage for local vertices
   - non-local vertices are hand out to the owning threads
   - vertices exchange – contention and lock-free queue structures
Parallel Construction of CSR Representation

Basic idea

1. Multi-core parallel state space generation
   - hash-based partitioning of the graph
   - local storage for local vertices
   - non-local vertices are hand out to the owning threads
   - vertices exchange – contention and lock-free queue structures

2. Concurrent parallel construction of CSR representation
   - computation of a unique integer number between 1 and $|V|$ for each vertex
   - when a cross transition is generated and stored to the CSR representation the number of target vertex is unknown
   - avoiding of multiple state space traversal
On-the-fly model checking computation

- multi-core state space generation
- one core oversees the communication with GPU device
On-the-fly model checking computation

- multi-core state space generation
- one core oversees the communication with GPU device
DiVinE-CUDA Workflow

On-the-fly model checking computation

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DiVinE-CUDA Workflow

On-the-fly model checking computation

- multi-core state space generation
- one core oversees the communication with GPU device

![Diagram showing DiVinE-CUDA Workflow](image-url)
On-the-fly model checking computation

- multi-core state space generation
- one core oversees the communication with GPU device
On-the-fly model checking computation

- multi-core state space generation
- one core oversees the communication with GPU device
Two Weaknesses of our Approach

2. Limited only to middle-size model checking problems

- CSR representation + MAP vectors has to fit to GPU memory

\[
\begin{pmatrix}
1 & 0 & 1 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 1
\end{pmatrix}
\]

\[
\begin{array}{c}
0 \quad 1 \quad 2 \quad 3 \quad 4 \\
\end{array}
\]

MC = (0 2 1 4 3 1 0 4)
MR = (0 2 4 5 6)
Two Weaknesses of our Approach

2. Limited only to middle-size model checking problems

- CSR representation + MAP vectors has to fit to GPU memory

\[
\begin{pmatrix}
1 & 1 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 1 \\
\end{pmatrix}
\]

\[Mc = (\begin{array}{cccccc}
0 & 2 & 1 & 4 & 3 & 1 \\
0 & 2 & 4 & 5 & 6 & \end{array})\]

\[Mr = (\begin{array}{cccc}
1 & 2 & 3 & 4 \\
0 & 2 & 1 & 4 & 3 & 1 & 0 & 4 \\
\end{array})\]

- GPU Memory consumption
  - Data stored on GPU
    - 12B per vertex (4B due to CSR + 8B due to MAP vectors)
    - 4B per edge (CSR)
  - 1 GB of GPU memory
    - 30 M of vertices, 150 M of edges (avg. outdegree 5)
    - 50 M of vertices, 100 M of edges (avg. outdegree 2)
Basic idea

- verification of the problems that fit the aggregate memory of multiple GPU devices
- split and distribute two data structures
  1. CSR representation of the graph
  2. vector of values associated with individual vertices

\[
M_i \times V = V'
\]
Two Proposed Partitioning

1. Only the CSR representation of the graph is partitioned
   - every GPU device keeps:
     - one part of the CSR representation of the graph
     - complete vector of values associated to individual vertices

1. GPU: \[ M_1 \]
   \[ V \times V' = i \]

2. GPU: \[ M_2 \]
   \[ V \times V' = j \]

3. GPU: \[ M_3 \]
   \[ V \times V' = k \]
Two Proposed Partitioning

CSR representation

Vector of MAP values
Two Proposed Partitioning

1. Only the CSR representation of the graph is partitioned
   - every GPU device keeps:
     - one part of the CSR representation of the graph
     - complete vector of values associated to individual vertices
   - foreign vertices – all vertices stored in foreign parts of the CSR representation

\[
\begin{align*}
M_1 & \quad V \quad V' \\
M_2 & \quad V \quad V' \\
M_3 & \quad V \quad V'
\end{align*}
\]
Two Proposed Partitioning

CSR representation

Vector of MAP values

1. GPU

2. GPU

3. GPU

(Foreign vertices)
Two Proposed Partitioning

1. Only the CSR representation of the graph is partitioned
   - every GPU device keeps:
     - one part of the CSR representation of the graph
     - complete vector of values associated to individual vertices

2. Also vector of values are partitioned
   - every GPU device keeps reduced vector
     - contains the values for all vertices that appear in the local
       CSR representation part

\[ \begin{align*}
1. & \text{GPU} \\
& M_1 \quad \times \quad V \quad V' \\
& i \left( \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right) \times \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right] = \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right] \\
2. & \text{GPU} \\
& M_2 \quad \times \quad V \quad V' \\
& j \left( \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right) \times \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right] = \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right] \\
3. & \text{GPU} \\
& M_3 \quad \times \quad V \quad V' \\
& k \left( \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right) \times \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right] = \left[ \begin{array}{c}
  \vdots \\
  \hline \\
  \vdots \\
\end{array} \right]
\end{align*} \]
Two Proposed Partitioning

CSR representation

Vector of MAP values
Two Proposed Partitioning

1. **Only the CSR representation of the graph is partitioned**
   - every GPU device keeps:
     - one part of the CSR representation of the graph
     - complete vector of values associated to individual vertices
   - foreign vertices – all vertices stored in foreign parts of the CSR representation

2. **Also vector of values are partitioned**
   - every GPU device keeps reduced vector
     - contains the values for all vertices that appear in the local CSR representation part
   - every GPU device keeps foreign vertices
     - target vertices of cross edges whose source vertices are stored in the local CSR representation part
Two Proposed Partitioning

CSR representation

Vector of MAP values

(Foreign vertices)

Milan Češka et al.  More CUDA Accelerated LTL Model Checking
Preparing Foreign Vertices Vectors

**Synchronisation during MAP computation**

- requires to exchange the values of the foreign vertices
- communication among GPU devices is realized through the host memory – maintains the complete vector of values
- first partitioning approach – efficient sequential read/write
Preparing Foreign Vertices Vectors

CSR representation

Vector of MAP values

(Foreign vertices)
Preparing Foreign Vertices Vectors

Synchronisation during MAP computation

- requires to exchange the values of the foreign vertices
- communication among GPU devices is realized through the host memory – maintains the complete vector of values
- first partitioning approach – efficient sequential read/write
- second partitioning approach – inefficient scattered read/write
Preparing Foreign Vertices Vectors

CSR representation

Vector of MAP values

( Foreign vertices )
Preparing Foreign Vertices Vectors

Synchronisation during MAP computation

- requires to exchange the values of the foreign vertices
- communication among GPU devices is realized through the host memory – maintains the complete vector of values
- first partitioning approach – efficient sequential read/write
- second partitioning approach – inefficient scattered read/write

Solution

- duplicate the values of the foreign vertices in the host memory
  - separate compacted vectors containing values for foreign vertices for particular CUDA devices
- create compacted vectors of values for foreign vertices on particular CUDA devices
Preparing Foreign Vertices Vectors

CSR representation

Vector of MAP values

Compacted vector

Foreign vertices

( )
Preparing Foreign Vertices Vectors

Synchronisation during MAP computation

- requires to exchange the values of the foreign vertices
- communication among GPU devices is realized through the host memory – maintains the complete vector of values
- first partitioning approach – efficient sequential read/write
- second partitioning approach – inefficient scattered read/write

Solution

- duplicate the values of the foreign vertices in the host memory
  - separate compacted vectors containing values for foreign vertices for particular CUDA devices
- create compacted vectors of values for foreign vertices on particular CUDA devices
  - map the foreign vertices in the CSR representation with their counterparts in the compacted vector
  - efficient compaction procedure on CUDA
• allocate a vector of size $2^i$ ($i$ is a small integer)
• CUDA kernels performing iteratively the following operations:
Compaction Procedure - Illustration

1. step

- store every foreign vertex \( v \) on the position \( v \& (2^{i-1} - 1) \)
- in case of conflicts for multiple vertices on some positions, we keep only the first vertex stored
2. step

- store conflicting vertices $v$ on the position $2^{i-1} + v \& (2^{i-1} - 1)$
- in case of conflicts for multiple vertices on some positions, we keep only the first vertex stored
3. step

- in case of conflicts we sequentially look for empty position from $2^i - 1 + v \& (2^i - 1 - 1) + 1$ to $2^i - 1 + v \& (2^i - 1 - 1) + i$
- if there are conflicts after $O(i)$ steps, we increment $i$ and repeat the procedure
• allocate a vector of size $2^i$

• CUDA kernels performing iteratively the following operations:
1. step

- store every foreign vertex \( v \) on the position \( v \&(2^{i-1} - 1) \)
- in case of conflicts for multiple vertices on some positions, we keep only the first vertex stored
2. step

- store conflicting vertices $v$ on the position $2^{i-1} + v \& (2^{i-1} - 1)$
- in case of conflicts for multiple vertices on some positions, we keep only the first vertex stored
Compaction Procedure - Illustration

3. step

- in case of conflicts we sequentially look for empty position from \(2^{i-1} + v \& (2^{i-1} - 1) + 1\) to \(2^{i-1} + v \& (2^{i-1} - 1) + i\)
- we have a compacted vector of the size \(2^i\) containing all foreign vertices exactly once
Sorting the vector

- values of allocated vector are initialized on zeroes
- external sorting procedure
Compaction Procedure - Illustration

Cutting off the prefix of zeroes
• map the foreign vertices with their counterparts in the sorted compacted vector

• CUDA implementation of binary search
Algorithm 1 \textit{MAP computation}

1: \textbf{while} \textit{globalChange} $\land \neg \text{acc\_found}$ \textbf{do}
2: \hspace{1em} \textit{foreignMAPs} $\leftarrow$ \textsc{Download}()
3: \hspace{1em} \textit{localChange} $\leftarrow$ false
4: \hspace{1em} \textbf{while} \textit{repropagate} $\land \neg \text{acc\_found}$ \textbf{do}
5: \hspace{2em} \textit{repropagate} $\leftarrow$ false
6: \hspace{2em} \textsc{mapKernel}(\textit{G}, \textit{localMAPs}, \textit{foreignMAPs})
7: \hspace{2em} \textsc{check}(\textit{repropagate}, \text{acc\_found})
8: \hspace{2em} \textit{localChange} $\leftarrow$ \textit{localChange} $\lor$ \textit{repropagate}
9: \hspace{1em} \textbf{end while}
10: \hspace{1em} \textsc{Upload}(\textit{localMAPs})
11: \hspace{1em} \textsc{VoteIn}(\textit{localChange})
12: \hspace{1em} \textsc{Rendezvous}()
13: \hspace{1em} \textit{globalChange} $\leftarrow$ \textsc{VoteOut}()
14: \textbf{end while}

MAP values of foreign vertices are received during the synchronisation with all the other GPU devices.
Algorithm 1 MAP computation

1: while globalChange ∧ ¬acc_found do
2:   foreignMAPs ← DOWNLOAD()
3:   localChange ← false
4:   while repropagate ∧ ¬acc_found do
5:     repropagate ← false
6:     MAPKernel(G, localMAPs, foreignMAPs)
7:     Check(repropagate, acc_found)
8:     localChange ← localChange ∨ repropagate
9:   end while
10:  UPLOAD(localMAPs)
11:  VOTEIN(localChange)
12:  RENDEZVOUS()
13:  globalChange ← VOTEOUT()
14: end while

Every single CUDA device computes the local fix-point using the mutable MAP values of local vertices and the constant MAP values of foreign vertices.
Algorithm 1 MAP computation

1: while $\text{globalChange} \land \neg \text{acc\textunderscore found}$ do
2:   $\text{foreignMAPs} \leftarrow \text{DOWNLOAD}()$
3:   $\text{localChange} \leftarrow \text{false}$
4:   while $\text{repropagate} \land \neg \text{acc\textunderscore found}$ do
5:     $\text{repropagate} \leftarrow \text{false}$
6:     MAPKernel($G$, localMAPs, foreignMAPs)
7:     CHECK(repropagate, acc\textunderscore found)
8:     $\text{localChange} \leftarrow \text{localChange} \lor \text{repropagate}$
9:   end while
10: $\text{UPLOAD}(\text{localMAPs})$
11: $\text{VOTEIN}(\text{localChange})$
12: $\text{RENDEZVOUS}()$
13: $\text{globalChange} \leftarrow \text{VOTEOUT}()$
14: end while

These steps are repeated until a global fix-point is found or accepting cycle is found.
Algorithm 1 \textit{MAP computation}

1: \textbf{while} globalChange \land \neg acc\_found \textbf{do}
2: \hspace{1em} foreignMAPs $\leftarrow$ \textsc{Download}()
3: \hspace{1em} localChange $\leftarrow$ false
4: \hspace{1em} \textbf{while} repropagate \land \neg acc\_found \textbf{do}
5: \hspace{2em} repropagate $\leftarrow$ false
6: \hspace{2em} \textsc{mapKernel}(G, localMAPs, foreignMAPs)
7: \hspace{2em} \textsc{check}(repropagate, acc\_found)
8: \hspace{2em} localChange $\leftarrow$ localChange \lor repropagate
9: \hspace{1em} \textbf{end while}
10: \hspace{1em} \textsc{Upload}(localMAPs)
11: \hspace{1em} \textsc{VoteIn}(localChange)
12: \hspace{1em} \textsc{Rendezvous}()
13: \hspace{1em} globalChange $\leftarrow$ \textsc{VoteOut}()
14: \textbf{end while}

If the local fix-point is found in zero iterations (no change after synchronisation step) workers vote for global termination.
Algorithm 1 \textit{MAP computation}

\begin{algorithm}
\begin{algorithmic}
\STATE \textbf{while} globalChange \land \neg acc\_found \textbf{do}
\STATE \hspace{1em} foreignMAPs \leftarrow \textsc{Download}()
\STATE \hspace{1em} localChange \leftarrow \text{false}
\STATE \hspace{1em} \textbf{while} repropagate \land \neg acc\_found \textbf{do}
\STATE \hspace{2em} repropagate \leftarrow \text{false}
\STATE \hspace{2em} \textsc{mapKernel}(G, localMAPs, foreignMAPs)
\STATE \hspace{2em} \textsc{Check}(repropagate, acc\_found)
\STATE \hspace{2em} localChange \leftarrow localChange \lor repropagate
\STATE \hspace{1em} \textbf{end while}
\STATE \hspace{1em} \textsc{Upload}(localMAPs)
\STATE \textsc{VoteIn}(localChange)
\STATE \textsc{Rendezvous}()
\STATE \textbf{globalChange} \leftarrow \textsc{VoteOut}()
\STATE \textbf{end while}
\end{algorithmic}
\end{algorithm}

If after a barrier operation the vote for termination is unanimous the algorithm terminates.
Redesign of OWCTY – Motivation

- OWCTY algorithm is more efficient than MAP algorithm on models without accepting cycle
Redesign of OWCTY – Motivation

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- OWCTY algorithm should prove more resistant to any improper ordering in CSR representation.
Reformulation of OWCTY Algorithm

- OWCTY algorithm comprises of alternating execution of
  - forward reachability
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- Reversed OWCTY algorithm
  - forward elimination – elimination of vertices without immediate successors (require just one step)
  - back reachability – less efficient (slower propagation)
DiVinE-CUDA Workflow

- multi-core state space generation
- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

![Diagram showing the workflow with mention of threads, OWCTY, MAP, and time.](image-url)
DiVinE-CUDA Workflow

- multi-core state space generation
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OWLCTY  MAP

3.
2.
1.

time
threads
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DiVinE-CUDA Workflow

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- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

OWCTY finished
cycle not found

interrupt
request

OWCTY
MAP
generator

1. 2. 3.

time
DiVinE-CUDA Workflow

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![DiVinE-CUDA Workflow Diagram]
DiVinE-CUDA Workflow

- multi-core state space generation
- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

OWCTY: Cycle not found
MAP: Cycle found

1. generator
2. 3.

ParaDiSe
Parallel & Distributed Systems Laboratory
DiVinE-CUDA Workflow

- multi-core state space generation
- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

OWCTY finished (enforced)  
new execution
DiVinE-CUDA Workflow

- multi-core state space generation
- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

\begin{figure}
\centering
\includegraphics[width=\textwidth]{diagram.png}
\caption{DiVinE-CUDA Workflow Diagram}
\end{figure}
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DiVinE-CUDA Workflow

- multi-core state space generation
- on-the-fly model checking computation
- two CUDA devices: concurrent execution of both algorithms

OWCTY found cycle early termination
Experimental Setting

Linux workstation with

- quad core AMD Phenom(tm) II X4 940 Processor @ 3GHz
- 8 GB DDR2 @ 1066 MHz RAM
- two NVIDIA GeForce GTX 280 GPU’s with 1GB of memory

- all the run-times in seconds
- CSR representation for models indicated by stars was created on a workstation with 32 GB RAM
- one core oversees the communication with CUDA device
Comparison of \texttt{DiVine} and \texttt{DiVine-CUDA}

<table>
<thead>
<tr>
<th>Valid Instances (models without accepting cycles)</th>
<th>CPU MAP</th>
<th>CPU OWCTY</th>
<th>CUDA MAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>State space generation</td>
<td>Green</td>
<td>Red</td>
<td>Green</td>
</tr>
<tr>
<td>Accepting cycle detection</td>
<td></td>
<td></td>
<td>40.9(14.4) speedup against MAP(OWCTY)</td>
</tr>
</tbody>
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<td>Green</td>
</tr>
<tr>
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<td></td>
<td></td>
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</tr>
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## Comparison of DiVINE and DiVINE-CUDA

<table>
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<th>Accepting Cycle Detection</th>
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<tr>
<td>CPU MAP</td>
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<td></td>
</tr>
<tr>
<td>CPU OWCTY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CUDA MAP</td>
<td></td>
<td>4.92(2.32) speedup against MAP(OWCTY)</td>
</tr>
<tr>
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<td></td>
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<tr>
<td>CPU MAP</td>
<td></td>
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<tr>
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<td></td>
<td></td>
</tr>
<tr>
<td>CUDA MAP</td>
<td></td>
<td>6.19(14.9) speedup against MAP(OWCTY)</td>
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Multi-core Acceleration of CSR Construction

- parallel CSR construction affects the ordering in CSR representation
- can lead to significant slowdown of the MAP algorithm
  - different number of calls to CUDA kernels
  - different memory access pattern
Employing Multiple CUDA Devices

verification of much larger model checking instances
- cannot be verified using the original CUDA algorithm
- fits the aggregate memory of multiple CUDA devices

slowdown of CUDA computation
- multiple CUDA computation requires the synchronisations
- 2nd method needs more time for initial phases

<table>
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<tr>
<th>Method</th>
<th>CUDA Computation</th>
<th>Initialisation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1st method</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2nd method</td>
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slowdown of CUDA computation
- multiple CUDA computation requires the synchronisations
- 2nd method needs more time for initial phases
- negligible with respect to the whole model checking procedure
Space Efficiency of Two Proposed Partitioning

- illustrate ability to efficiently utilise space when increasing number of CUDA devices is employed
- average over all tested models
- 2nd method is significantly better for partitioning of a wide variety of graphs
Comparison of CUDA MAP and CUDA OWCTY

Invalid instances (models with accepting cycles)

- algorithms have almost same times on most of the instances
- on some instances (e.g. peterson 2) the MAP algorithm falls behind both the OWCTY algorithms significantly

<table>
<thead>
<tr>
<th>Models (seq. total time: MAP/OWCTY)</th>
<th>CPU cores</th>
<th>CSR time</th>
<th>CUDA MAP</th>
<th>CUDA OWCTY</th>
<th>CUDA OWCTY REVERSE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>CUDA time</td>
<td>total time</td>
<td>CUDA time</td>
</tr>
<tr>
<td>peterson 2 (173/404)</td>
<td>1</td>
<td>25.7</td>
<td>4.0</td>
<td>30.5</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>17.4</td>
<td>4.3</td>
<td>22.5</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>12.5</td>
<td>0.6</td>
<td>13.8</td>
<td>1.2</td>
</tr>
</tbody>
</table>

- CUDA accelerated MAP algorithm deeply depends on the ordering in CSR representation
- CUDA accelerated OWCTY algorithm is more resistant to slowdown caused by improper ordering
Comparison of CUDA MAP and CUDA OWCTY

Valid instances (models without accepting cycles)

<table>
<thead>
<tr>
<th></th>
<th>1 core</th>
<th></th>
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<tr>
<td></td>
<td>MAP</td>
<td>OWCTY</td>
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<td></td>
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<tr>
<td></td>
<td>(2.6% of total)</td>
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<table>
<thead>
<tr>
<th></th>
<th>2 cores</th>
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<th></th>
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<th></th>
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</tr>
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Milan Češka et al.  More CUDA Accelerated LTL Model Checking 18.1, 2011 30 / 33
**Conclusion**

**Successful redesign of MAP algorithm**

- significant GPU acceleration of LTL Model Checking
- DiVinE-CUDA – tool for CUDA Accelerated Model Checking
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Exhaustive experimental evaluation
Current and Future Work

Improve the performance of multi CUDA algorithms

- on-the-fly property
- new techniques allowing efficient utilization of GPU clusters
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CUDA accelerated state space generation

- crucial for CUDA accelerated model checking
- [Edelkam et al. SPIN’10]
  - CUDA accelerated
    - checking of transitions enabledness
    - generating the successors
  - nonsignificant speed up due to CPU duplicate detection
- necessity of CUDA accelerated duplicate detection
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CUDA acceleration of other graph problems

- strongly connected component decomposition
  [Barnat et al. IPDPS’11]
- mean weight cycles
Thank you for your attention.

More information:

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