cycles per instruction : LXC : avrora (uncontrolled) and h2 (controlled), "best" pinning
<table>
<thead>
<tr>
<th>Cycles per instruction</th>
<th>LXC</th>
<th>h2 (uncontrolled)</th>
<th>avrora (controlled)</th>
<th>&quot;best&quot; pinning</th>
</tr>
</thead>
</table>

[Diagram showing various line graphs and data distributions.]

[Further details and analysis not visible in the image.]
cycles per instruction \[1\]: LXC : luindex (uncontrolled) and scalac (controlled), "best" pinning

staircase trace time \[s\]

L3 cache misses \[6/s\]: LXC : luindex (uncontrolled) and scalac (controlled), "best" pinning
cycles per instruction [1] : LXC : scalac (uncontrolled) and specs (controlled), "best" pinning

staircase trace time [s]