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# NSWI101

## FIRST HOMEWORK ASSIGNMENT

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The goal of the assignment is to model the MESI cache coherency protocol in Promela. The description of the protocol itself can be found at [http://en.wikipedia.org/wiki/MESI\\_protocol](http://en.wikipedia.org/wiki/MESI_protocol). The model should contain a process type `cpu` modeling a CPU. This process type should be instantiated several times each representing a CPU. The `cpu` process should in a cycle write and read values from and to random places in the memory (simulating a general program) using a cache as a speed optimization (assume that the cache can be accessed faster than the main memory). The cache is then used according to the MESI coherence protocol. The model should be checked for interesting properties (e.g., the state of each cache is always coherent) – think of as many interesting properties as possible, but verify at least those expressing correctness of the algorithm.

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### EXAMPLE PARAMETRIZATION (YOU ARE FREE TO MODIFY IT)

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The size of global memory is 4 bytes.

The number of `cpus` is 2.

The size of the cache of each `cpu` is 1 byte.

The values stored in the cache and memory are 0 and 1.

The `cpus` communicate via a shared variable (while using a channel is another option).

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### NOTES

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1. If you want to access local variables of processes inside LTL formulae, do not put them inside the process, but make them global.