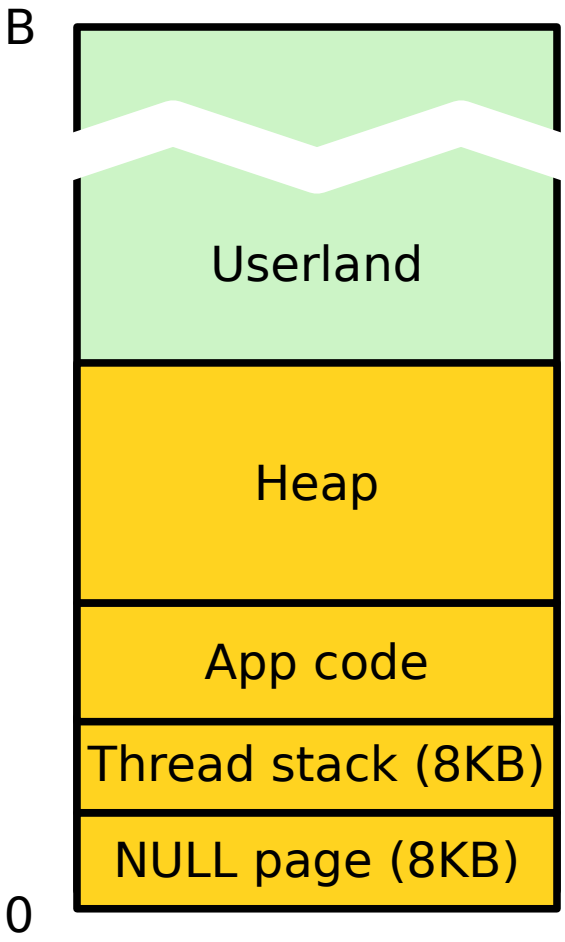
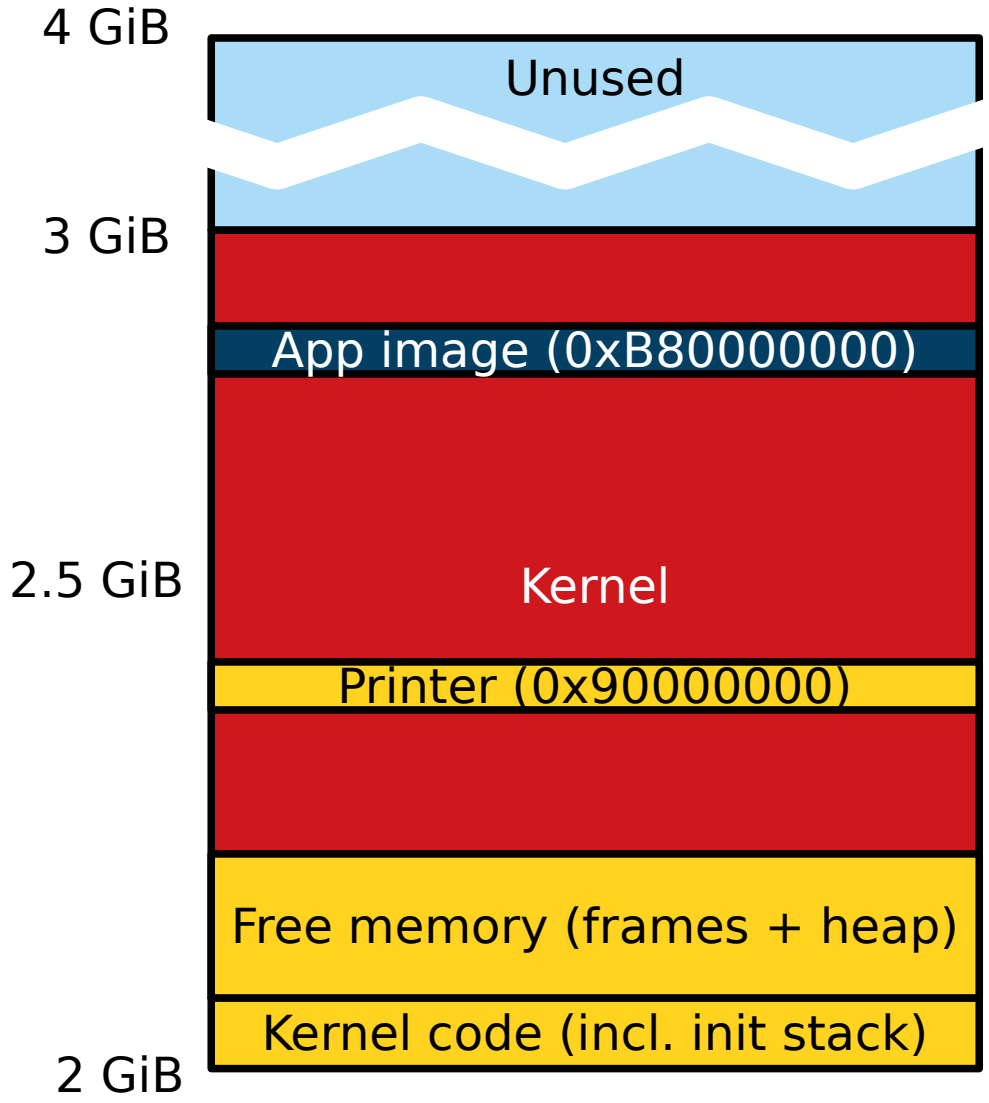
NSWI200

Virtual Memory Management Milestone M05

Virtual Address Space

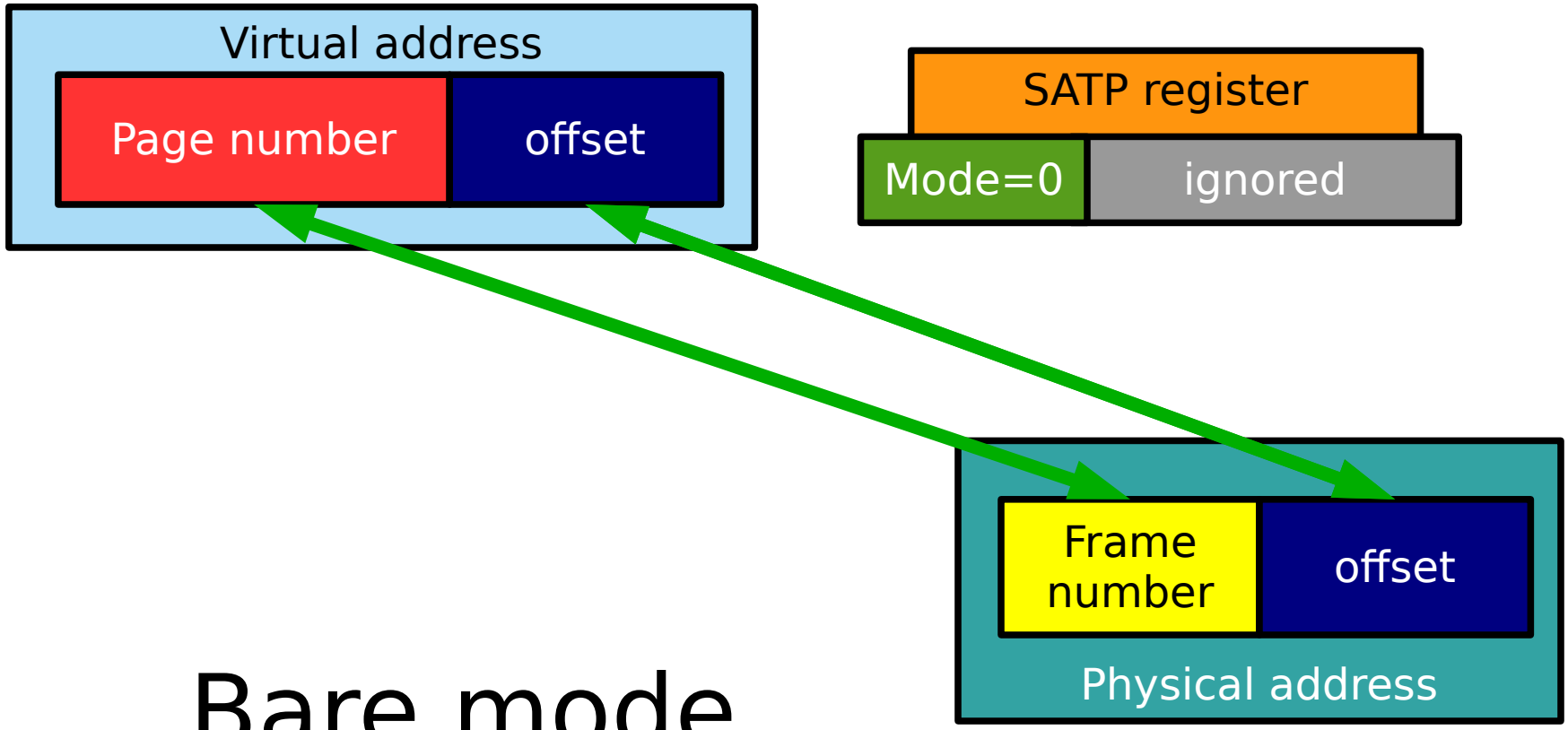
Notes:
- loader not shown (CPU-specific)
- userspace etc. in M06





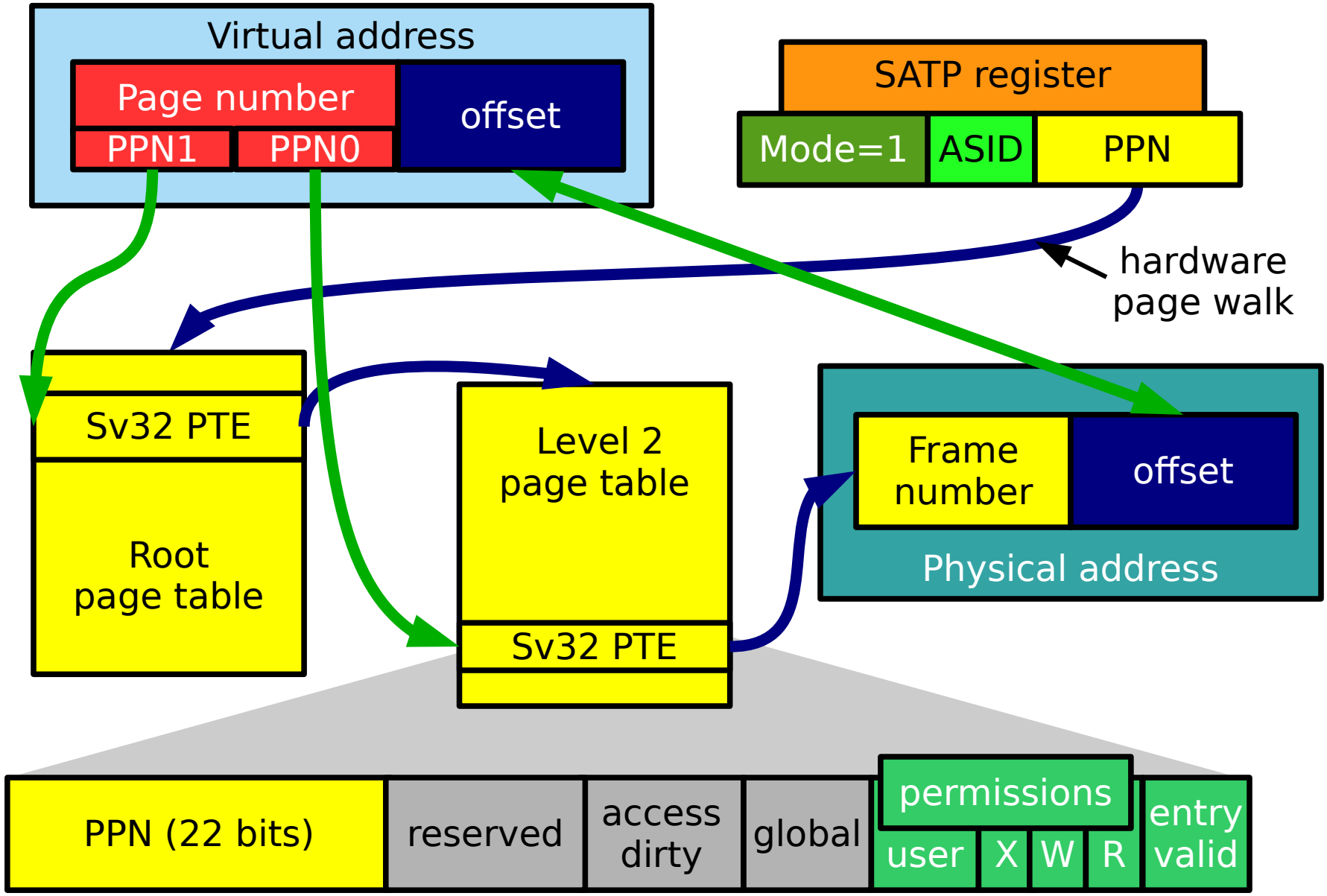
RISC-V

RISC-V (Mode=Bare)



Bare mode translation (used before M05)

RISC-V (Mode=Sv32)



MIPS R4000

Virtual Address Space

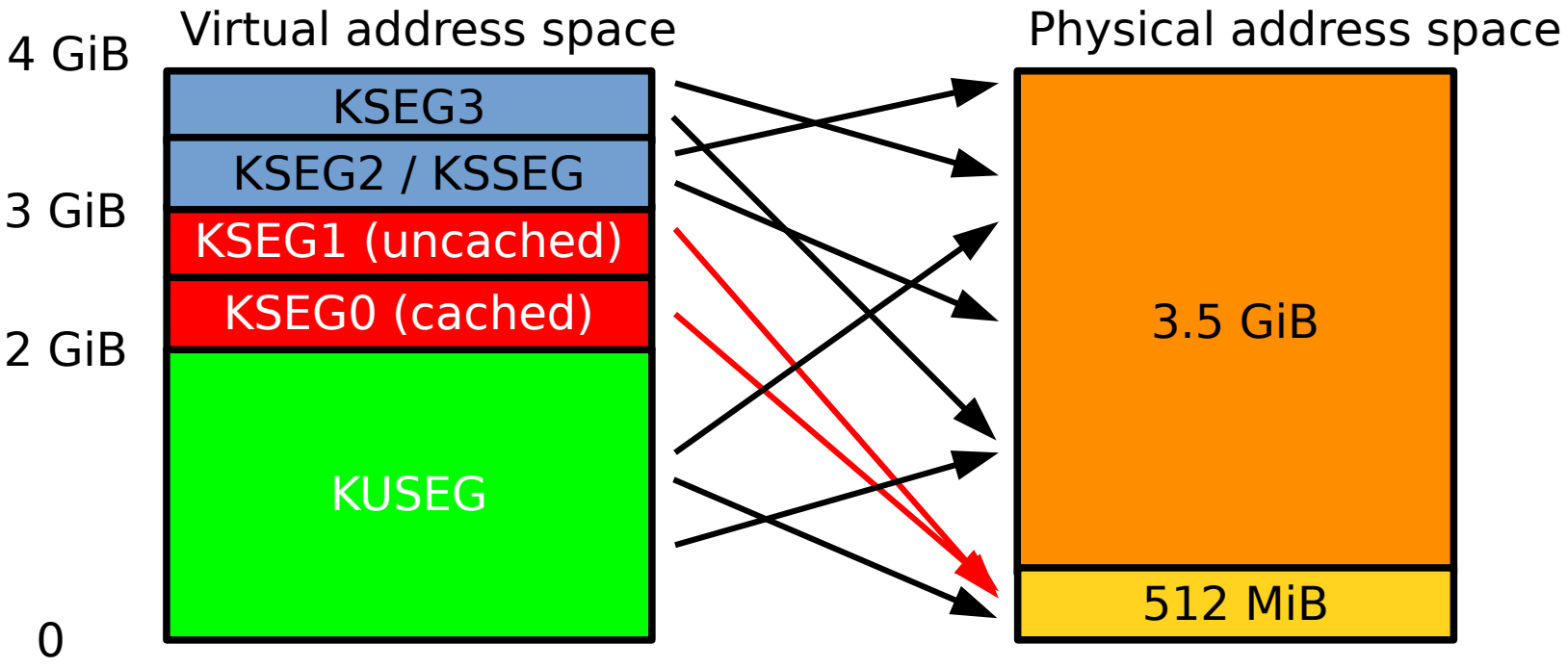
Hard-wired segments (top 3 bits)

- KSEG0, KSEG1 – identity mapping
- KUSEG, KSEG2, KSEG3 – TLB

unprivileged, TLB mapped

privileged, identity mapped

privileged, TLB mapped



Translation Lookaside Buffer (TLB)

- 48 records (software-managed), each entry contains:
  - Page size mask (from 4 KiB up to 16 MiB)
  - Two virtual pages (stored as VPN2)
  - Two frame addresses (FPN)
  - ASID
  - Extra bits: global, dirty, valid
- Translation
  - Match entry based on ASID (EntryHi) and virtual address
  - On miss
    - TLB exception (usually “refill”)
    - Entry added (OS searches its data structures, e.g. hierarchical page tables)
    - Instruction restarted

MIPS R4000 TLB